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EEC 180B

Lab 1 Report

Exercises:

1. What are tsu, tco, tpd, and th? What do each of these times signify?

Times are included in attached sheet.

tsu = setup time

tco = clock to output delay

tpd = propagation delay

th = hold time

2. What is the critical path of your circuit and the maximum frequency of operation?

The critical path of the circuit is through the adder, MUX, and Count register as seen on the schematic. The maximum frequency of operation was measured to be 378.93 MHz.

3. Examine and print the schematic of your synthesized circuit. Explain how the up-counting and the down-counting functions are implemented. Verify the logic used for counting down.

Two adders are used with a static 1 or -1 added to the current Count value. The switch determines whether up or down counting will be used because it is connected to the select bit of the 2-to-1 MUX.

4. Compare the timing simulation results with the results from the Quartus II Classic Timing Analyzer Tool. Are they in agreement?

Yes, we can see a propagation delay of roughly 10 ns on the LEDG wave. Using a cursor, I measured the tpd to be equal to ~9 ns while Quartus gave a time of 10.108 ns.

5. Print a portion of your timing simulation waveform for your report.

Attached.

6. Print the Power Analyzer Summary for your lab report.

Attached.